

B: Amendments to The Claims:

What is claimed is:

1 1. (Cancelled)

1 Claim 2. (Amended) An apparatus comprising:  
2 a processor handling an I/O request in an I/O operation;  
3 main storage controlled by the processor for storing data;  
4 one or more I/O devices for sending data to or receiving data from said main  
5 storage;  
6 a vector mechanism operable to register I/O requests by said devices to send or  
7 receive data from said main storage;  
8 a dispatcher operable to poll said vector mechanism to determine if there is an  
9 outstanding I/O request; and  
10 an override bit having a first condition when an immediate interrupt is to be sent to  
11 said processor for handling an I/O request from said I/O device(s), and a second condition  
12 when said dispatcher is to poll said vector mechanism to determine if there is an  
13 outstanding I/O request, said override bit being set to its first condition or reset to its  
14 second condition by said processor, and  
15 further comprising a Target Delay Interval (TDI) register containing a TDI value for  
16 determining when the vector mechanism should not be polled by said dispatcher and an  
17 interrupt given to said processor, and wherein said override bit, when in its first  
18 condition, overrides said TDI value and drives an immediate interrupt to said processor.

1 Claim 3. (Amended) The apparatus of claim 2 wherein said main storage is  
2 divided into multiple partitions, with each partition having a vector mechanism operable  
3 to register I/O requests by said devices to send or receive data from that partition of main  
4 storage, each partition having an associated override bit for that partition, and said  
5 processor is a hypervisor for setting the override bit for that partition when said hypervisor  
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is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

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Claim 4. (Original). The apparatus of claim 3 further comprising one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the override bit of one partition when that partition does not have a CPU assigned to it.

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Claim 5. (Cancelled)

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Claim 6. (Cancelled)

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Claim 7. (Cancelled)

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Claim 8. (Cancelled)

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Claim 9. (Cancelled)

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Claim 10. (Cancelled)

Claim 11. (Cancelled)

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Claim 12. (Cancelled)

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Claim 13. (Cancelled)

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Claim 14. (Amended) A method for controlling the transfer of data in a data processing system having a processor handling an I/O request in an I/O operation, main storage controlled by the processor for storing data, and one or more I/O devices for sending data to or receiving data from said main storage, said method comprising:  
registering in a vector mechanism, I/O requests by said devices to send or receive data from said main storage;

11 polling with a dispatcher, said vector mechanism to determine if there is an  
12 outstanding I/O request; and  
13 sending an immediate interrupt to said processor when an override bit has a first  
14 condition for handling an I/O request from said I/O device(s), or polling with said  
15 dispatcher, said vector mechanism to determine if there is an outstanding I/O request when  
16 said override bit is in a second condition, and  
17 wherein said data processing further includes a Target Delay Interval (TDI) register  
18 containing a TDI value for determining when the vector mechanism should not be polled  
19 by said dispatcher and an interrupt given to said processor, said method further comprising  
1 overriding said TDI value and driving an immediate interrupt to said processor when said  
2 override bit is in its first condition.  
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5 Claim 15. (Currently Amended) The method of claim ~~13~~ 14 wherein said  
6 main storage is divided into multiple partitions, with each partition having a vector  
7 mechanism operable to register I/O requests by said devices to send or receive data from  
8 that partition of main storage, each partition having an associated override bit for that  
1 partition, and said processor is a hypervisor, said method further comprising setting by  
2 said hypervisor the override bit for that partition when said hypervisor is to handle an  
3 immediate interrupt rather than polling by said dispatcher for that partition.  
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5 Claim 16. (Original) The method of claim 15 wherein said data processing  
6 system further includes one or more central processing units (CPUs) assignable by said  
1 hypervisor to one or more of said partitions, said method further comprising setting by  
said hypervisor, the override bit of one partition when that partition does not have a CPU  
1 assigned to it.

1 Claim 17. (Cancelled)

1 Claim 18. (Cancelled)  
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3 Claim 19. (Cancelled)

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5 Claim 20. (Amended) A program product for controlling the transfer of data in a  
6 data processing system having a processor handling an I/O request in an I/O operation,  
7 main storage controlled by the processor for storing data, and one or more I/O devices for  
8 sending data to or receiving data from said main storage, said program product  
9 comprising:

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11 a computer readable medium having recorded thereon computer readable program  
12 code means for performing the method comprising:

13 registering in a vector mechanism, I/O requests by said devices to send or receive  
14 data from said main storage;

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16 polling with a dispatcher, said vector mechanism to determine if there is an  
17 outstanding I/O request; and

18 sending an immediate interrupt to said processor when an override bit has a first  
19 condition for handling an I/O request from said I/O device(s), or polling with said  
20 dispatcher, said vector mechanism to determine if there is an outstanding I/O request when  
21 said override bit is in a second condition, and

1 wherein said data processing further includes a Target Delay Interval (TDI) register  
2 containing a TDI value for determining when the vector mechanism should not be polled  
3 by said dispatcher and an interrupt given to said processor, said method further comprising  
4 overriding said TDI value and driving an immediate interrupt to said processor when said  
5 override bit is in its first condition.  
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Claim 21. (Currently Amended) The program product of claim ~~19~~ 20 wherein  
said main storage is divided into multiple partitions, with each partition having a vector  
mechanism operable to register I/O requests by said devices to send or receive data from  
1 that partition of main storage, each partition having an associated override bit for that  
2 partition, and said processor is a hypervisor, said method further comprising setting by  
3 said hypervisor the override bit for that partition when said hypervisor is to handle an  
4 immediate interrupt rather than polling by said dispatcher for that partition.  
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1 Claim 22. (Original) The program product of claim 21 wherein said data processing system further includes one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said method further comprising setting by said hypervisor, the override bit of one partition when that partition does not have a CPU assigned to it.

Claim 23. (Cancelled)